PROGRAMMABLE MEMORY CELL USING CHARGE
TRAPPING IN A GATE OXIDE

5   This application is a Continuation of U.S. Application No. 09/924,659, filed August 8, 2001, which is a Divisional of U.S. Application No. 09/383,804, filed on August 26, 1999, now U.S. Patent No. 6,521,958, both of which are incorporated herein by reference.

10   **Field of the Invention**

      The present invention relates generally to semiconductor integrated circuits and, more particularly, to MOSFET technology for programmable address decode and correction.

15   **Background of the Invention**

      Many electronic products need various amounts of memory to store information, e.g. data. One common type of high speed, low cost memory includes dynamic random access memory (DRAM) comprised of individual DRAM cells arranged in arrays. DRAM cells include an access transistor, e.g a metal oxide

20   semiconducting field effect transistor (MOSFET) coupled to a capacitor cell. Programmable address decode circuits and buffers are needed in conjunction with the DRAM array to allow faulty rows and/or columns in a memory array to be replaced by functional redundant rows and/or columns. An example of a redundancy repair scheme is shown in U.S. patent # 5,324,681 issued Lowrey on

25   June 28, 1994. Another is provided in U.S. patent # 4,051,354 issued Choate on September 27, 1997. Another is provide in U.S. patent # 5,327,380 issued Kersh III on July 5, 1994.

      With the increasing array density of successive generations of DRAM chips, the attractiveness of merging other functions onto the chip, e.g. programmable

30   address decode logic, also increases. However, any successful merged technology product must be cost competitive with the existing alternative of combining separate

chips at the card or package level, each being produced with independently optimized technologies. Any significant addition of process steps to an existing DRAM technology in order to provide added functions such as high speed logic, SRAM or EEPROM becomes rapidly cost prohibitive due to the added process

5 complexity cost and decreased yield. Thus, there is a need for a means of providing additional functions on a DRAM chip with little or no modification of the DRAM optimized process flow.

Programmable address decode circuits conventionally employ one time programmable switches in such decode circuits. Fuses and antifuses, present in

10 circuits peripheral to the DRAM chips, are one method for constructing address decode logic. The fuse or antifuse integrally combines the functions of a switching element which makes the interconnection and a programming element which stores the state of the switching element, either "off" or "on," e.g. a blown or unblown fuse. A fuse or antifuse, however, has the disadvantage of not being

15 reprogrammable. This single-time programmability makes the antifuse difficult to test and unsuitable for a large class of applications where reprogrammability is required. The fuse or antifuse further has the disadvantage on not being fabricated according to the DRAM process flow.

Micron Technology, Inc. taught in U.S. patent # 5,324,681 which issued to

20 Lowrey et al. on June 28, 1994, that one time programmable (OTP) memory cells formed as MOSFETs could be used to replace laser/fuse programmable memory cells for applications such as OTP repair of DRAMs using redundant rows and columns of DRAM memory cells and OTP selection of options on a DRAM (such as fast page mode (FPM) or extended data out (EDO)). One of the key advantages

25 of that capability is the ability to program the OTP memory cells after the DRAM memory chip is packaged (a decided advantage over previous solutions). However, the invention in the Lowrey patent still has the disadvantage of single-time programmability.

Another approach to solving the programmable switching problem is described in U.S. patent number 5,764,096, which issued to Lipp et al. on June 9, 1998. U.S. patent number 5,764,096 provides a general purpose non-volatile, reprogrammable switch, but does not achieve the same using the commonality in basic DRAM cell structure. Thus, the Lipp patent does not achieve the desired result of providing non-volatile memory functions on a DRAM chip with little or no modification of the DRAM process flow.

Still another alternative to programmable interconnects, e.g. logic switching circuits, uses a metal oxide semiconductor field effect transistor (MOSFET) as the switching element. The MOSFET is controlled by the stored memory bit of a programming element. Most commonly, this programming element is a dynamic random access memory (DRAM) cell. Such DRAM based field programmable gate arrays (FPGAs) are reprogrammable and use a DRAM process flow, but have a disadvantage in that the programming of the switching elements is lost whenever power is turned off. A separate, non-volatile memory cell must be used to store the programmed pattern on power down, and the FPGA must be reprogrammed each time the device is powered back up. This need again increases the fabrication complexity and requires significant additional chip surface space.

Thus, there is a need for DRAM technology compatible non-volatile memory cells which can be used as programmable logic arrays (PLAs). It is desirable that such DRAM technology non-volatile memory cells be fabricated on a DRAM chip with little or no modification of the DRAM process flow. It is further desirable that such DRAM technology non-volatile memory cells operate with lower programming voltages than that used by conventional non-volatile memory cells, yet still hold sufficient charge to withstand the effects of parasitic capacitances and noise due to circuit operation.

Summary of the Invention

The above mentioned problems for creating DRAM technology compatible non-volatile memory cells as well as other problems are addressed by the present invention and will be understood by reading and studying the following

5   specification. This disclosure teaches structures and methods using MOSFET devices as re-programmable elements in memory address decode circuits in a DRAM integrated circuit. The structures and methods use the existing process sequence for MOSFET's in DRAM technology.

In particular, an illustrative embodiment of the present invention includes a

10   non-volatile, reprogrammable circuit switch. The circuit switch includes a metal oxide semiconductor field effect transistor (MOSFET) in a substrate. The MOSFET has a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by a gate oxide. A wordline is coupled to the gate of the MOSFET. A first transmission line is coupled to the

15   source region. A second transmission line is coupled to the drain region. The MOSFET is a programmed MOSFET having a charge trapped in the gate oxide adjacent to the source region such that the channel region has a first voltage threshold region ($Vt1$) and a second voltage threshold region ($Vt2$). The $Vt2$ is adjacent to the source region and $Vt1$ is adjacent to the drain region. In the present

20   invention, $Vt2$ has a greater voltage threshold than $Vt1$ due the charge trapped in the gate oxide adjacent to the source region. Hence, the programmed MOSFET of the present invention conducts significantly less current than a conventional MOSFET, particularly at low voltage drain voltages.

In another embodiment of the present invention, the relatively small change

25   in the programmed MOSFET, in comparison to flash or EEPROM devices, is compensated for by using the novel circuit switch in a cross coupled latch. Array, system, and programming method embodiments are similarly included in the scope of the present invention.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention.

5   The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

10   Figure 1A is a block diagram of a metal oxide semiconductor field effect transistor (MOSFET) in a substrate according to the teachings of the prior art.

Figure 1B illustrates the MOSFET of Figure 1A operated in the forward direction showing some degree of device degradation due to electrons being trapped in the gate oxide near the drain region over gradual use.

15   Figure 1C is a graph showing the square root of the current signal (Ids) taken at the drain region of the conventional MOSFET versus the voltage potential (VGS) established between the gate and the source region.

Figure 2A is a diagram of a programmed MOSFET which can be used as a circuit switch, or non volatile, reprogrammable switch according to the teachings of

20   the present invention.

Figure 2B is a graph plotting the current signal (Ids) detected at the drain region versus a voltage potential, or drain voltage, (VDS) set up between the drain region and the source region (Ids vs. VDS).

Figure 2C is a diagram suitable for explaining the method by which the

25   MOSFET of the circuit switch, or non-volatile, reprogrammable switch 201 of the present invention can be programmed to achieve the embodiments of the present invention.

Figure 3A is a schematic diagram illustrating a latch according to the teachings of the present invention.

Figure 3B is a logic diagram illustrating an operational embodiment of the latch of Figure 3A which has a programmed MOSFET according to the teachings of the present invention.

Figure 3C is a logic diagram illustrating another operational embodiment of the latch of Figure 3A which has a programmed MOSFET according to the teachings of the present invention.

Figure 4 is a block diagram illustrating an integrated circuit according to the teachings of the present invention.

Figure 5 is a block diagram illustrating an electronic system according to the teachings of the present invention.

Description of the Preferred Embodiments

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term conductor is understood to include semiconductors, and the term insulator is

defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims

5 are entitled.

According to the teachings of the present invention, normal MOSFETs can be programmed by operation in the reverse direction and utilizing avalanche hot electron injection to trap electrons in the gate oxide of the MOSFET. When the programmed MOSFET is subsequently operated in the forward direction the

10 electrons trapped in the oxide are near the source and cause the channel to have two different threshold voltage regions. The novel programmed MOSFETs of the present invention conduct significantly less current than conventional MOSFETs, particularly at low drain voltages. These electrons will remain trapped in the gate oxide unless negative gate voltages are applied. The electrons will not be removed

15 from the gate oxide when positive or zero gate voltages are applied. Erasure can be accomplished by applying negative gate voltages and/or increasing the temperature with negative gate bias applied to cause the trapped electrons to be re-emitted back into the silicon channel of the MOSFET.

There are two components to the effects of stress and hot electron injection.

20 One component includes a threshold voltage shift due to the trapped electrons and a second component includes mobility degradation due to additional scattering of carrier electrons caused by this trapped charge and additional surface states. When a conventional MOSFET degrades, or is "stressed," over operation in the forward direction, electrons do gradually get injected and become trapped in the gate oxide

25 near the drain. In this portion of the conventional MOSFET there is virtually no channel underneath the gate oxide. Thus the trapped charge modulates the threshold voltage and charge mobility only slightly.

Figure 1A is a block diagram of a metal oxide semiconductor field effect transistor (MOSFET) 101 in a substrate 100 as exists in the prior art. The

MOSFET 101 includes a source region 102, a drain region 104, a channel region 106 in the substrate 100 between the source region 102 and the drain region 104. A gate 108 is separated from the channel region 108 by a gate oxide 110. A sourceline 112 is coupled to the source region 102. A bitline 114 is coupled to the

5   drain region 104. A wordline 116 is coupled to the gate 108.

In conventional operation, a drain to source voltage potential (Vds) is set up between the drain region 104 and the source region 102. A voltage potential is then applied to the gate 108 via a wordline 116. Once the voltage potential applied to the gate 108 surpasses the characteristic voltage threshold (Vt) of the MOSFET a

10   channel 106 forms in the substrate 100 between the drain region 104 and the source region 102. Formation of the channel 106 permits conduction between the drain region 104 and the source region 102, and a current signal (Ids) can be detected at the drain region 104.

In operation of the conventional MOSFET of Figure 1A, some degree of

15   device degradation does gradually occur for MOSFETs operated in the forward direction by electrons 117 becoming trapped in the gate oxide 110 near the drain region 104. This effect is illustrated in Figure 1B. However, since the electrons 117 are trapped near the drain region 104 they are not very effective in changing the MOSFET characteristics.

20   Figure 1C illustrates this point. Figure 1C is a graph showing the square root of the current signal (Ids) taken at the drain region versus the voltage potential (VGS) established between the gate 108 and the source region 102. The change in the slope of the plot of $\sqrt{Ids}$ versus VGS represents the change in the charge carrier mobility in the channel 106.

25   In Figure 1C, ΔVT represents the minimal change in the MOSFET's threshold voltage resulting from electrons gradually being trapped in the gate oxide 110 near the drain region 104, under normal operation, due to device degradation. This results in a fixed trapped charge in the gate oxide 110 near the drain region 104. Slope 1 represents the charge carrier mobility in the channel 106 for Figure

1A having no electrons trapped in the gate oxide 110. Slope 2 represents the charge mobility in the channel 106 for the conventional MOSFET of Figure 1B having electrons 117 trapped in the gate oxide 110 near the drain region 104. As shown by a comparison of slope 1 and slope 2 in Figure 1C, the electrons 117

5   trapped in the gate oxide 110 near the drain region 104 of the conventional MOSFET do not significantly change the charge mobility in the channel 106.

Figure 2A is a diagram of a programmed MOSFET which can be used as a circuit switch, or non volatile, reprogrammable switch 201 according to the teachings of the present invention. As shown in Figure 2A the circuit switch 201

10   includes a MOSFET in a substrate 200 which has a first source/drain region 202, a second source/drain region 204, and a channel region 206 between the first and second source/drain regions, 202 and 204. In one embodiment, the first source/drain region 202 includes a source region 202 for the MOSFET and the second source/drain region 204 includes a drain region 204 for the MOSFET.

15   Figure 2A further illustrates a gate 208 separated from the channel region 206 by a gate oxide 210. A first transmission line 212 is coupled to the first source/drain region 202 and a second transmission line 214 is coupled to the second source/drain region 204. In one embodiment, the first transmission line includes a sourceline 212 and the second transmission line includes a bit line 214.

20   As stated above, circuit switch 201 is comprised of a programmed MOSFET. This programmed MOSFET has a charge 217 trapped in the gate oxide 210 adjacent to the first source/drain region 202 such that the channel region 206 has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2) in the channel 206. In one embodiment, the charge 217 trapped in the gate

25   oxide 210 adjacent to the first source/drain region 202 includes a trapped electron charge 217.

Figure 2A illustrates the Vt2 in the channel 206 is adjacent the first source/drain region 202 and that the Vt1 in the channel 206 is adjacent the second source/drain region 204. According to the teachings of the present invention, Vt2

has a higher voltage threshold than Vt1 due to the charge 217 trapped in the gate oxide 217 adjacent to the first source/drain region 202.

Figure 2B is a graph plotting a current signal (Ids) detected at the second source/drain region 204 versus a voltage potential, or drain voltage, (VDS) set up between the second source/drain region 204 and the first source/drain region 202 (Ids vs. VDS). In one embodiment, VDS represents the voltage potential set up between the drain region 204 and the source region 202. In Figure 2B, the curve plotted as D1 represents the conduction behavior of a conventional MOSFET which is not programmed according to the teachings of the present invention. The curve D2 represents the conduction behavior of the programmed MOSFET, described above in connection with Figure 2A, according to the teachings of the present invention. As shown in Figure 2B, for a particular drain voltage, VDS, the current signal (Ids2) detected at the second source/drain region 204 for the programmed MOSFET (curve D2) is significantly lower than the current signal (Ids2) detected at the second source/drain region 204 for the conventional MOSFET which is not programmed according to the teachings of the present invention. Again, this is attributed to the fact that the channel 206 in the programmed MOSFET of the present invention has two voltage threshold regions and that the voltage threshold, Vt2, near the first source/drain region 202 has a higher voltage threshold than Vt1 near the second source/drain region due to the charge 217 trapped in the gate oxide 217 adjacent to the first source/drain region 202.

Figure 2C is a diagram suitable for explaining the method by which the MOSFET of the circuit switch, or non-volatile, reprogrammable switch 201 of the present invention can be programmed to achieve the embodiments of the present invention. As shown in Figure 2C the method includes programming the MOSFET in a reverse direction. Programming the MOSFET in the reverse direction includes applying a first voltage potential V1 to a drain region 204 of the MOSFET. In one embodiment, applying a first voltage potential V1 to the drain region 204 of the

MOSFET includes grounding the drain region 204 of the MOSFET as shown in Figure 2C. A second voltage potential V2 is applied to a source region 202 of the MOSFET. In one embodiment, applying a second voltage potential V2 to the source region 202 includes applying a high positive voltage potential (VDD) to the

5 source region 202 of the MOSFET, as shown in Figure 2C. A gate potential VGS is applied to a gate 208 of the MOSFET. In one embodiment, the gate potential VGS includes a voltage potential which is less than the second voltage potential V2, but which is sufficient to establish conduction in the channel 206 of the MOSFET between the drain region 204 and the source region 202. As shown in

10 Figure 2C, applying the first, second and gate potentials (V1, V2, and VGS respectively) to the MOSFET creates a hot electron injection into a gate oxide 210 of the MOSFET adjacent to the source region 202. In other words, applying the first, second and gate potentials (V1, V2, and VGS respectively) provides enough energy to the charge carriers, e.g. electrons, being conducted across the channel 206

15 that, once the charge carriers are near the source region 202, a number of the charge carriers get excited into the gate oxide 210 adjacent to the source region 202. Here the charge carriers become trapped.

In one embodiment of the present invention, the method is continued by subsequently operating the MOSFET in the forward direction in its programmed

20 state. Accordingly, the method includes re-coupling a sourceline 212 to the source region 202. A bit line 214 is re-coupled to the drain region. And, a gate potential is applied to the gate 208 by a wordline 216 such that a conduction channel is formed between the source and the drain regions.

Now in its programmed state, the conduction channel 206 of the MOSFET

25 will have a first voltage threshold region (Vt1) adjacent to the drain region 204 and a second voltage threshold region (Vt2) adjacent to the source region 202, as explained and described in detail in connection with Figure 2A. According to the teachings of the present invention, the Vt2 has a greater voltage threshold than the Vt1 due to the hot electron injection 217 into a gate oxide 210 of the MOSFET

adjacent to the source region 202.

Figure 3A is a schematic diagram illustrating a latch 300 according to the teachings of the present invention. Latch 300 includes a pair of cross coupled inverters, 301 and 302 respectively. Each inverter, 301 and 302, includes a first

5 conduction type MOSFET, M1 and M2 respectively. In one embodiment, the first conduction type MOSFET includes an n-channel metal oxide semiconductor (NMOS) transistor. Each inverter, 301 and 302, includes a second conduction type MOSFET, M3 and M4 respectively. In one embodiment, the second conduction type MOSFETs include p-channel metal oxide semiconductor (PMOS) transistors.

10 Each MOSFET has a first source/drain region, a second source/drain region, a channel region between the first and the second source/drain regions, and a gate separated from the channel by a gate oxide. In one embodiment of the present invention, the first source/drain region of each MOSFET includes a source region and the second source/drain region includes a drain region.

15 As shown in Figure 3A, the drain region 304 of MOSFET M1 is coupled to the drain region 308 of MOSFET M3 at node 1. Similarly, the drain region 306 of MOSFET M2 is coupled to the drain region 310 of MOSFET M4 at node 2. In the novel latch 300 shown in Figure 3A, a source region 326 of MOSFET M1 is coupled to a first voltage potential at node 3. A source region 328 of MOSFET M2

20 is similarly coupled to the first voltage potential at node 3. Further a source region 330 of MOSFET M3 is coupled to a second voltage potential at node 4 and a source region 332 of MOSFET M4 is also coupled to the second voltage potential at node 4. In one embodiment, the first voltage potential at node 3 includes a ground potential. In one embodiment, the second voltage potential at node 4

25 includes a power supply voltage.

A first transmission line 312 is coupled to node 1. The first transmission line 312 is further coupled via node 1 to the gates 316 and 318 of MOSFETs M2 and M4 of inverter 302, or first inverter 302. At node 1, the first transmission line 312 is coupled to the drain regions 304 and 308 of MOSFETs M1 and M3 of

inverter 301, or second inverter 301. A second transmission line 314 is coupled to node 2. The second transmission line 314 is further coupled via node 2 to the gates 320 and 322 of MOSFETs M1 and M3 of second inverter 301. At node 2, the second transmission line 314 is coupled to the drain regions 306 and 310 of

5   MOSFETs M2 and M4 of first inverter 302.

In one embodiment, the latch 300 includes an input line 324 operatively coupled to the first transmission line 312 and the second transmission line 314. In the embodiment shown in Figure 3A, the input line 324 is coupled to first transmission line 312 by MOSFET M5 and the input line 324 is coupled to the

10   second transmission line 314 by MOSFET M6. The input line 324 couples to a gate 334 of MOSFET M5 and to a gate 336 of MOSFET M6.

According to the teachings of the present invention, at least one of the MOSFETs, M1, M2, M3, and M4 in latch 300 is a programmed MOSFET as described and explained in detail above in connection with Figures 2A-2C. The at

15   least one programmed MOSFET includes a non-volatile, reprogrammable MOSFET. As described in connection with Figures 2A-2C the programmed MOSFET has a charge trapped in a gate oxide adjacent to the first source/drain region such that a channel region for the programmed MOSFET has a first voltage threshold region (Vt1) and a second voltage threshold region (Vt2). In one

20   embodiment, the charge trapped in the gate oxide adjacent the first source/drain region includes a trapped electron charge.

The second voltage threshold region (Vt2) in the channel in the programmed MOSFET is adjacent to the first source/drain region of the programmed MOSFET. The first voltage threshold region (Vt1) in the channel in

25   the programmed MOSFET is adjacent to the second source/drain region of the programmed MOSFET. According to the teachings of the present invention, the Vt2 has a higher voltage threshold than the Vt1. As described and explained in detail in connection with Figures 2A-2C, the programmed MOSFET conducts significantly less current than the unprogrammed MOSFETs of latch 300,

particularly at low drain voltages.

Figure 3B is a logic diagram illustrating an operational embodiment of latch 300 which has a programmed MOSFET according to the teachings of the present invention. In the example of Figure 3B, MOSFET M1 has been programmed as

5   described and explained in detail in connection with Figures 2A-2C. In operation, first transmission line 312 and second transmission line 314 are initially balanced at some positive voltage potential value. Next, a positive voltage potential is applied to input line 324 of Figure 3A. In one embodiment, the voltage potential applied to input line 324 is greater than the voltage potential initially applied to balance the

10   first transmission line 312 and the second transmission line 314.

The voltage potential applied to input line 324 enables, or turns "on," transistors M5 and M6, shown as NMOS transistors in Figure 3A, permitting conduction through these transistors such that first transmission line 312 is coupled to node 1 and second transmission line 314 is coupled to node 2. The positive

15   voltage potential applied to node 1 and node 2 is coupled to the gates 318 and 322 of transistors M4 and M3, shown as PMOS transistors in Figure 3A. Here, the positive voltage potential applied to nodes 1 and 2 is not too large and allows transistors M4 and M3 to turn "on". The positive voltage potential applied to node 1 and node 2 is similarly coupled to the gates 316 and 320 of transistors M2 and

20   M1, shown as NMOS transistors in Figure 3A. Here, the positive voltage potential serves to turn "on" transistor M2.

However, due to the programmed state of MOSFET M1, MOSFET M1 conducts significantly less current than MOSFET M1 would in an unprogrammed state despite the positive voltage applied to it's gate 320. Therefore an output

25   voltage on the first transmission line 312 is significantly changed and approaches to voltage of node 4. In other words, if the initial voltage applied to first transmission line 312 is represented by the value A/2, then the final output voltage on the first transmission line 312 after sensing is approximately the voltage potential A, or the voltage of node 4.

Conversely, since the unprogrammed NMOS M2 was turned "on" and conducts normally, an output voltage on the second transmission line 314 is significantly changed where the conduction through transistor M2 couples the second transmission line 314 to a different voltage potential at node 3. Thus, if the initial voltage applied to second transmission line 314 is represented by the value A/2, then the final output voltage on the second transmission line 314 after sensing has a new value represented by the value A*.

Figure 3C is a logic diagram illustrating another operational embodiment of latch 300 which has a programmed MOSFET according to the teachings of the present invention. In the example of Figure 3C, MOSFET M2 has been programmed as described and explained in detail in connection with Figures 2A-2C. In operation, first transmission line 312 and second transmission line 314 are initially balanced at some positive voltage potential value. Next, a positive voltage potential is applied to input line 324 of Figure 3A. In one embodiment, the voltage potential applied to input line 324 is larger than the voltage potential initially applied to balance the first transmission line 312 and the second transmission line 314.

The voltage potential applied to input line 324 enables, or turns "on," transistors M5 and M6, shown as NMOS transistors in Figure 3A, permitting conduction through these transistors such that first transmission line 312 is coupled to node 1 and second transmission line 314 is coupled to node 2. The positive voltage potential applied to node 1 and node 2 is coupled to the gates 318 and 322 of transistors M4 and M3, shown as PMOS transistors in Figure 3A. Here, the positive voltage potential applied to nodes 1 and 2 is not too large and allows transistors M4 and M3 to turn "on".

The positive voltage potential applied to node 1 and node 2 is also coupled to the gates 316 and 320 of transistors M2 and M1, shown as NMOS transistors in Figure 3A. Here, the positive voltage potential serves to turn "on" transistor M1. However, due to the programmed state of MOSFET M2, MOSFET M2 conducts

significantly less current than MOSFET M2 would in an unprogrammed state despite the positive voltage applied to it's gate 316. Therefore an output voltage on the second transmission line 314 is significantly changed and becomes the voltage of node 4. In other words, if the initial voltage applied to second transmission line 314 is represented by the value A/2, then the final output voltage on the second transmission line 314 after sensing is approximately the voltage potential A, or the voltage of node 4.

Conversely, since the unprogrammed NMOS M1 was turned "on" and conducts normally, an output voltage on the first transmission line 312 is significantly changed where the conduction through transistor M1 couples the first transmission line 312 to a different voltage potential at node 3. Thus, if the initial voltage applied to first transmission line 312 is represented by the value A/2, then the final output voltage on the first transmission line 312 after sensing has a new value represented by the value A*.

One of ordinary skill in the art will understand upon reading this disclosure that transistors M3 and M4 in latch 300 can similarly be programmed to comprise a programmed MOSFET, or non-volatile reprogrammable MOSFET according to the teachings of the present invention. Depending on which MOSFET in latch 300 has been programmed, the asymmetry in latch 300 will cause the latch 300 to flip one way or the other. Two distinctly different output configurations are possible.

The latch illustrated in Fig. 3A will have two distinctly different states depending upon the programming of the transistors M1 and M2. Two complementary outputs lines 312 and 314 are available for reading the programmed state of the latch, the latch can be addressed by using the line 324 and applying a large positive voltage to turn on transistors M5 and M6. One possible configuration of the latch is illustrated in Fig. 3B, inputting a positive voltage, A, on line 324 results in a complementary output, A*, on line 314 and a non-inverted output, A, on line 312. The other possible configuration of the latch is shown in Fig. 3C, inputting a positive voltage, A, on line 324 results in a non-inverted

output, A, on line 314 and an inverted complementary output, A*, on line 312. In practice for instance only one output line might be utilized in which case an input, A, on line 324 can result in either an output, A, or A* on line 314 depending upon the programming of the transistors M1 and M2 in the latch.

5   Figure 4 is a block diagram illustrating an integrated circuit 400 according to the teachings of the present invention. In one embodiment according to the teachings of the present invention, the integrated circuit 400 includes an address decoder portion for a memory. As shown in Figure 4, the integrated circuit 400 includes a programmable decoder 401. According to the teachings of the present

10   invention, the programmable decoder 401 includes an array of latches arranged in a matrix of rows and columns. The array of latches in the programmable decoder 401 includes non-volatile, reprogrammable latches having a programmed MOSFET as described and explained in detail in connection with Figures 3A-3C.

      According to the teachings of the present invention, the array of latches in

15   programmable decoder 401 are disposed at the intersection of a number of first transmission lines, shown collectively as 403, and a number of second transmission lines, shown collectively as 405. The number of first transmission lines 403 couple an address driver 406 to the array of latches in the programmable decoder 401. In one embodiment, the number of first transmission lines 403 includes a number of

20   address input lines 403. The number of second transmission lines 405 couple a number of row drivers 408 and at least one redundant row driver 409 to the array of latches in the programmable decoder 401. In one embodiment, the number of second transmission lines 405 includes a number of output lines 405.

      According to the teachings of the present invention, the latches within the

25   array of latches in programmable decoder 401 can be programmed to have two distinct outputs as explained in connection with Figures 3A-3C. Depending on which MOSFET in a given latch is programmed, the asymmetry in the latch will cause the latch to flip one way or the other for two distinctly different output configurations. These programmed output configurations for the array of latches in

the programmable decoder constitute a programmed logic array (PLA). The amount of signaling necessary to upset, or flip, the latch is similar to the considerations in the design of DRAM sense amplifiers. Thus, a 50 millivolt (mV) signal, or offset, in the threshold voltages for the MOSFETs of the latch will upset

5   the latch. This insures programming in the PLA such that each latch will always output the same one of the two possible bistable states upon selection and activation.

As one of ordinary skill in the art will understand upon reading this disclosure, the two distinct output states can be used to allow faulty rows and/or

10   columns in a memory array to be replaced by functional redundant rows and/or columns. For example, according to the teachings of the present invention, programmed latches in the array of latches in the programmable decoder 401 can be used to un-select a first set 411 of the second transmission lines 405 which couple to a primary row driver, e.g. row driver 408, and to instead select a second set 412

15   of the second transmission lines 405 which couple to a redundant row driver 409. Thus, the PLAs in the programmable decoder formed by latches with programmed MOSFETs according to the teachings of the present invention function in an equivalent manner to PLAs constructed from EEPROM devices. Under the present invention, however, the PLAs are formed according to a DRAM process

20   technology which avoids the added complexity and cost associated with creating PLAs with EEPROM devices.

Figures 2C, 3A and 4, are illustrative of a method embodiment for performing address decoding in a memory according to the teachings of the present invention. The method includes coupling a number of address lines 403 to a

25   number of latches 300 in an array of latches in programmable decoder 401. The method includes coupling a number of output lines 405 to the number of latches 300 in the array of latches in the programmable decoder 401 wherein each latch is disposed at an intersection of an address line 403 and an output line 405. At least one of the number of latches 300 is programmed as described in connection with

Figures 3A-3C.

The programmed latch 300 includes a MOSFET programmed to be a non-volatile, reprogrammable MOSFET as described in connection with Figures 2A-2C, using hot electron injection to trap a charge in the gate oxide adjacent to the

5   source region in the programmed MOSFET. According then to the teachings of the present invention, the latch having the programmed MOSFET is operated in the forward direction with the conduction channel of the programmed MOSFET having a first voltage threshold region (Vt1) adjacent to the drain region and having a second voltage threshold region (Vt2) adjacent to the source region of the

10   MOSFET. Operating the latch in the forward direction includes operating the programmed MOSFET in the forward direction where Vt2 has a greater voltage threshold than the Vt1 due to the charge trapped in the gate oxide adjacent to the source region of the programmed MOSFET.

Further, performing address decoding in a memory according to the

15   teachings of the present invention includes coupling an output line from at least one of the number of latches to a row driver when the at least one of the number of latches is in an unprogrammed state, and coupling the output line to a redundant row driver when the at least one of the number of latches is in a programmed state. Also, performing address decoding in a memory according to the teachings of the

20   present invention includes unprogramming a latch in a programmed state. Unprogramming the latch in a programmed state includes removing a charge trapped in a gate oxide region adjacent to a source region in a MOSFET of the latch in a programmed state.

Programming the latches of the present invention, e.g. writing to a

25   MOSFET in the latch, by channel hot electron injection and avalanche injection proceeds in a manner similar to hot electron injection and programming of Flash memory devices. The MOSFET to be programmed is turned on. For example, the latch 300 in Figure 3A is selected using input line 324. The first transmission line 312 and the second transmission line 314 are controlled such that one transmission

line is used to set the gate voltages in a first inverter of the latch 300 and the other transmission line is used to turn up the drain voltage across the MOSFET to be programmed in a second inverter of the latch 300. Extra lines and circuits (not shown) can be used in peripheral circuits as necessary to accomplish this.

5   As with Flash memory devices programming is easily accomplished in second time frames or less.

Erasing the latches of the present invention, e.g. erasing a programmed MOSFET in a programmed latch, is accomplished by applying a large negative gate voltage to get tunneling of the electrons trapped in the oxide back to the silicon in a

10   manner similar to tunnel erase of Flash memory devices. For example, with silicon on insulator (SOI) MOSFETs this could most easily be accomplished by biasing the desired first or second transmission lines connected to the gates in one inverter of the latch 300 negative and/or the p-type well positive. For bulk silicon MOSFET devices extra transistors might be required to disconnect some of the connections if

15   parasitic diodes exist which can become forward biased.

Erase times are exponential functions of both voltage and temperature. A thick oxide device, e.g. having a gate oxide thickness of approximately 200 Angstroms (Å), takes a relatively long time to erase at room temperature, with a gate voltage of -12V. However, current flash memory technology uses gate

20   voltages of -10V on approximately 100 Å thick gate oxides, which is a much higher electric field. Because of the exponential dependence on electric field in tunneling processes, this results in a much shorter erase time. In one embodiment, the erase time issue can also be reduced by increasing the temperature of the MOSFET while a negative gate voltage is applied.

25   Figure 5 is a block diagram illustrating an electronic system according to the teachings of the present invention. As shown in Figure 5, the electronic system includes a memory 510 and a processor 520 coupled to the memory by a system bus 530. In one embodiment, the processor and memory are located on a single semiconductor chip. The memory 510 includes a programmable decoder which has

at least one latch having a programmed MOSFET according to the teachings of the present invention and as explained and described in detailed in connection with Figure 4.

5   Conclusion

Thus, the ability to provide PLA capability on a DRAM chip according to a DRAM optimized process flow has been shown by the present invention. Advantages of the present invention include no extra processing steps to produce the non-volatile, reprogrammable MOSFETs. The size of the non-volatile,

10   reprogrammable MOSFETs of the present invention, and the latches they are used in scale and shrink as the DRAM technology process margins are reduced. The non-volatile, reprogrammable MOSFETs of the present invention, and the latches they are used in operate at the same voltages as for conventional DRAM. Voltage multipliers are utilized for the programming and erase functions of the MOSFETs

15   according to the teachings of the present invention. The voltage multipliers used for erase/programming are located in the peripheral circuit areas in the lay out of the DRAM and do not damage other device or circuits since they are not in close proximity. The non-volatile, reprogrammable MOSFETs of the present invention, and the latches they are used in, can be reprogrammable 5-10 times and should

20   retain data for 12 years (4x life of average PC). Further the process yields associated with constructing the non-volatile, reprogrammable MOSFETs of the present invention, and the latches they are used in are near 100%, since they are fabricated according to a standard DRAM process flow.

It is to be understood that the above description is intended to be

25   illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.